

74AHC574; 74AHCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Product data sheet

1. General description

The 74AHC574; 74AHCT574 are high-speed Si-gate CMOS devices and are pin compatible with Low Power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC574; 74AHCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable (\overline{OE}) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When \overline{OE} is LOW the contents of the 8 flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The 74AHC574; 74AHCT574 is functionally identical to the 74AHC564; 74AHCT564, but has non-inverting outputs. The 74AHC574; 74AHCT574 is functionally identical to the 74AHC374; 74AHCT374, but has a different pinning.

2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- 3-state non-inverting outputs for bus orientated applications
- 8-bit positive, edge-triggered register
- Independent register and 3-state buffer operation
- Common 3-state output enable input
- For 74AHC574 only: operates with CMOS input levels
- For 74AHCT574 only: operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC574D 74AHCT574D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC574PW 74AHCT574PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHC574BQ 74AHCT574BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

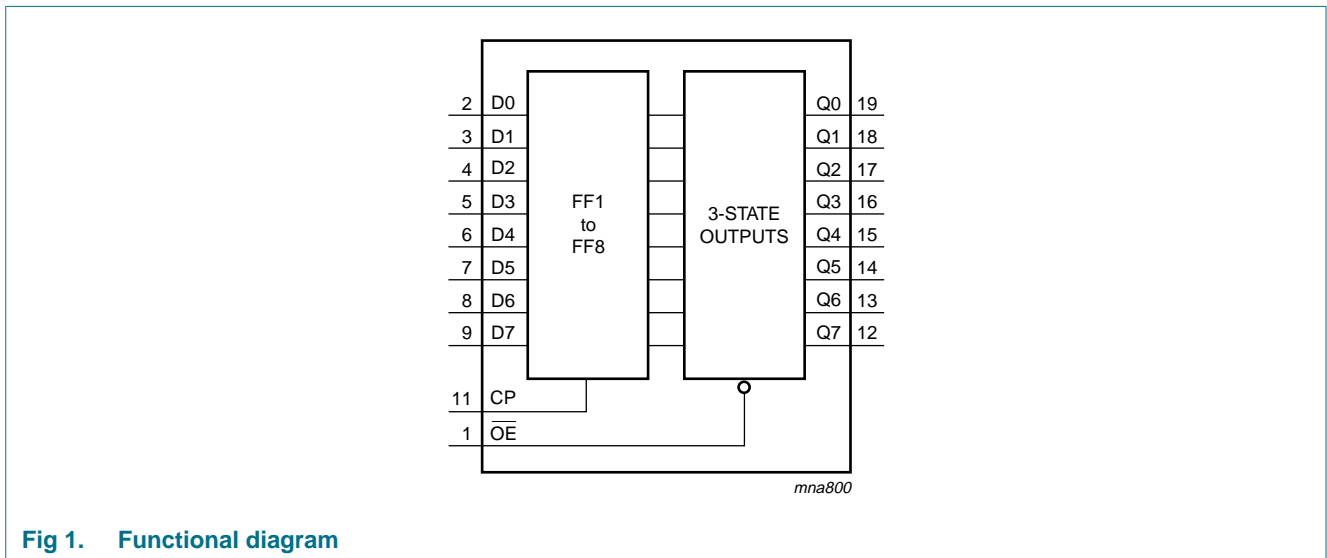


Fig 1. Functional diagram

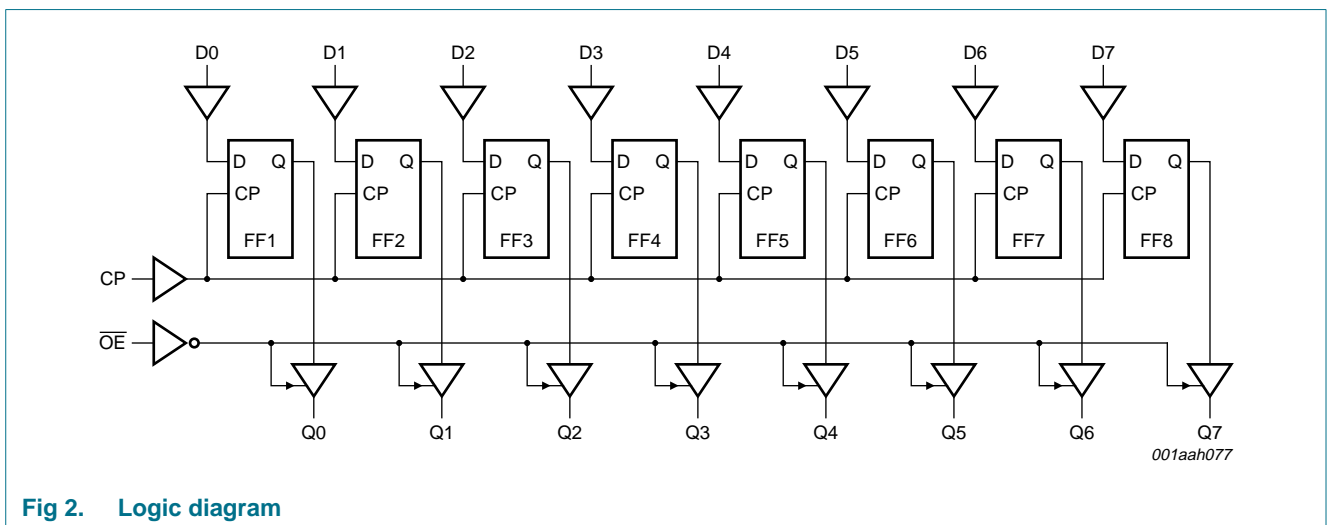


Fig 2. Logic diagram

6. Functional description

Table 3. Function table^[1]

Operating mode	Input			Internal flip-flop	Output Qn
	\overline{OE}	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;
 L = LOW voltage level;
 l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;
 Z = high-impedance OFF-state;
 ↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
	SO20 package		[2] -	500	mW
	TSSOP20 package		[3] -	500	mW
	DHVQFN20 package		[4] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] P_{tot} derates linearly with 8 mW/K above 70 °C.
 [3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 [4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC574			74AHCT574			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC574										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.0	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF
For type 74AHCT574										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; I _O = 0 A; V _O = V _{CC} or GND; other pins at V _{CC} or GND	-	-	±0.25	-	±2.5	-	±10.0	μA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF

Table 7. Dynamic characteristics ...continued
GND = 0 V. For test circuit see [Figure 10](#).

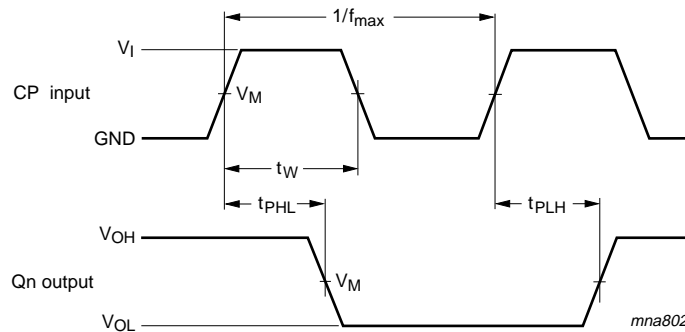
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	Dn to CP; see Figure 8								
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	3.5	-	-	3.5	-	3.5	-	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	3.0	-	-	3.0	-	3.0	-	ns
t _h	hold time	Dn to CP; see Figure 8								
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	1.5	-	-	1.5	-	1.5	-	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	1.5	-	-	1.5	-	1.5	-	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC}	^[3]	-	10	-	-	-	-	pF
For type 74AHCT574										
t _{pd}	propagation delay	CP to Qn; see Figure 7		^[2]						
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.4	8.6	1.0	10.0	1.0	11.0	ns
		C _L = 50 pF	-	6.3	10.6	1.0	12.0	1.0	13.5	ns
t _{en}	enable time	$\overline{\text{OE}}$ to Qn; see Figure 9								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.3	9.0	1.0	10.5	1.0	11.5	ns
		C _L = 50 pF	-	6.1	11.0	1.0	12.5	1.0	14.0	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to Qn; see Figure 9		^[2]						
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.3	9.0	1.0	10.5	1.0	11.5	ns
		C _L = 50 pF	-	6.2	10.1	1.0	11.5	1.0	13.0	ns
f _{max}	maximum frequency	CP; see Figure 7								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	130	180	-	110	-	110	-	MHz
		C _L = 50 pF	85	115	-	75	-	75	-	MHz
t _w	pulse width	CP; HIGH or LOW; see Figure 7								
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	5.0	-	-	5.5	-	5.5	-	ns
t _{su}	set-up time	Dn to CP; see Figure 8								
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	3.0	-	-	3.5	-	3.5	-	ns

Table 7. Dynamic characteristics ...continued
 GND = 0 V. For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t_h	hold time	Dn to CP; see Figure 8 $V_{CC} = 4.5\text{ V to }5.5\text{ V};$ $C_L = 50\text{ pF}$	1.5	-	-	1.5	-	1.5	-	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}; f = 1\text{ MHz};$ $V_I = \text{GND to }V_{CC}$	[3]	-	12	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5.0\text{ V}$).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.

10.1 Waveforms

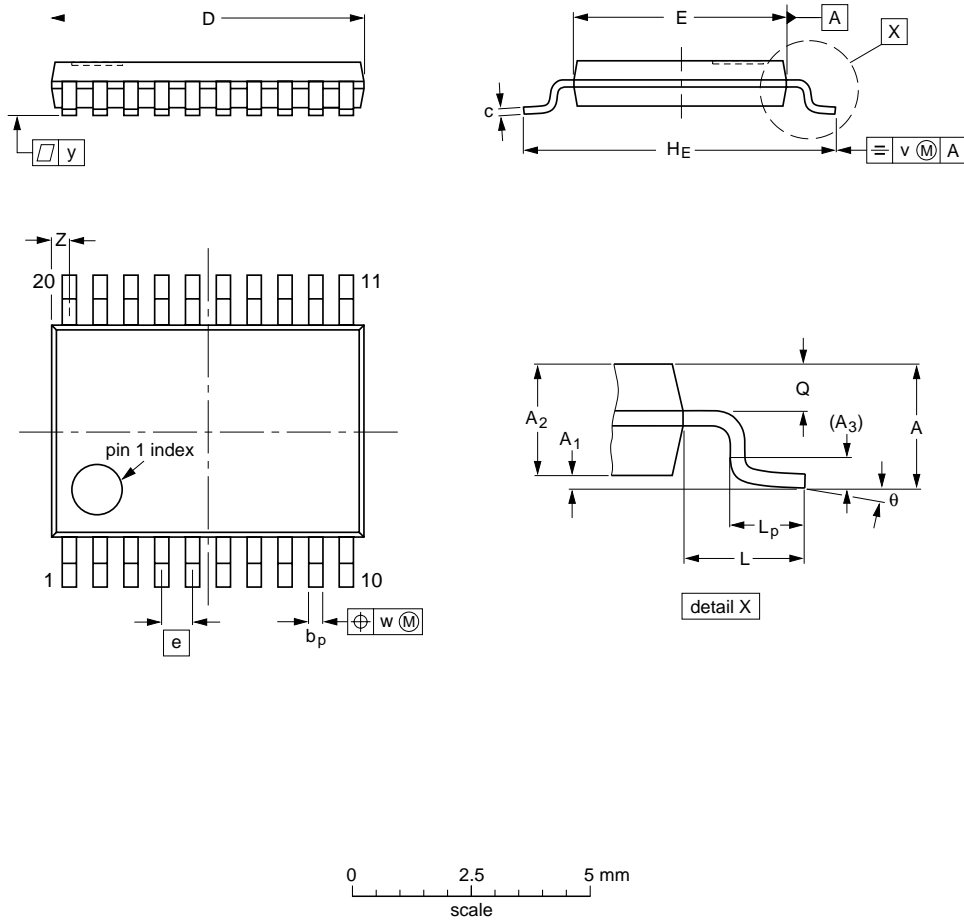


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay input (CP) to output (Qn), clock input (CP) pulse width and the maximum frequency (CP)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT360-1		MO-153		

Fig 12. Package outline SOT360-1 (TSSOP20)